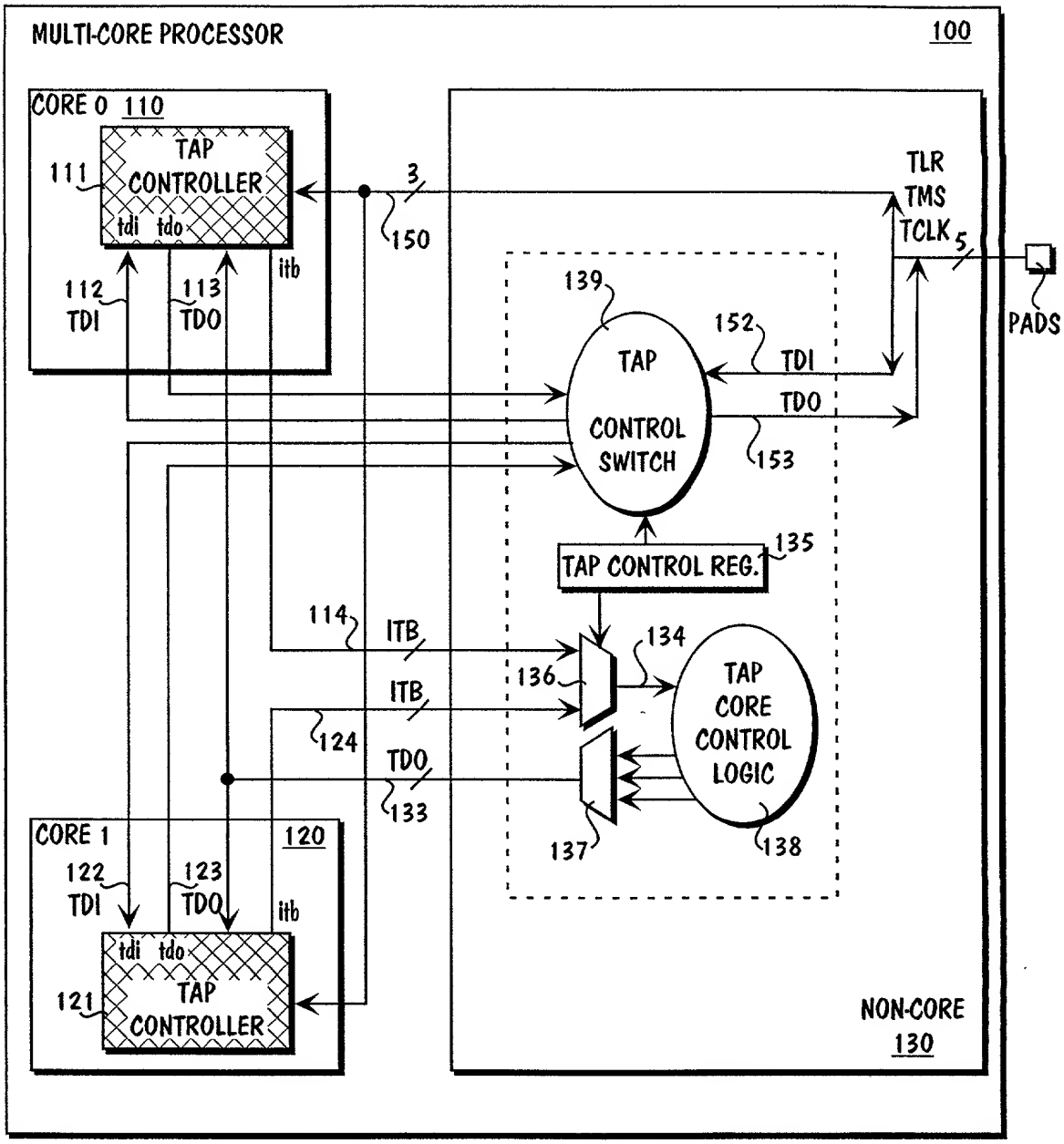

MULTI-CORE PROCESSOR
100
CORE 0 110
TAP CONTROLLER
111
tdi tdo
itb
112 TDI
113 TDO
3
150
TLR
TMS
TCLK
5
PADS
139
TAP CONTROL SWITCH
152 TDI
TDO
153
TAP CONTROL REG.
135
114 ITB
134
136
TAP CORE CONTROL LOGIC
ITB
124
TDO
133
137
138
CORE 1
120
122 TDI
123 TDO
itb
tdi tdo
TAP CONTROLLER
121
NON-CORE
130

FIG. 1

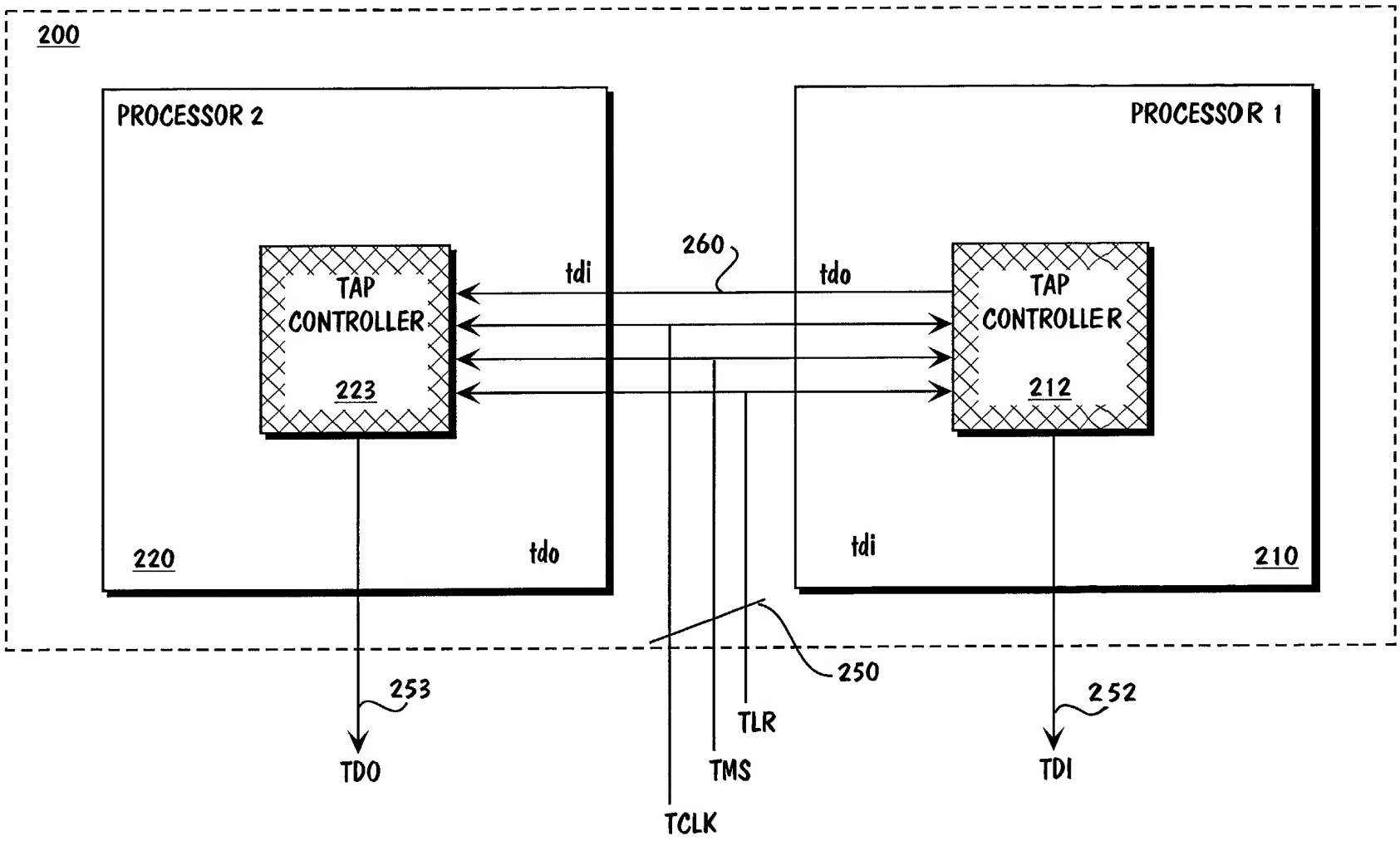

200
PROCESSOR 2
PROCESSOR 1
TAP CONTROLLER
223
TAP CONTROLLER
212
260
tdi
tdo
tdo
tdi
220
210
253
250
252
TDO
TLR
TMS
TDI
TCLK

FIG. 2

FIG. 3a

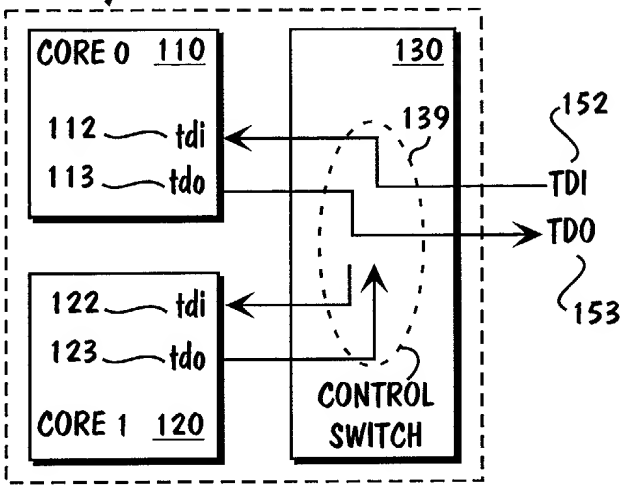
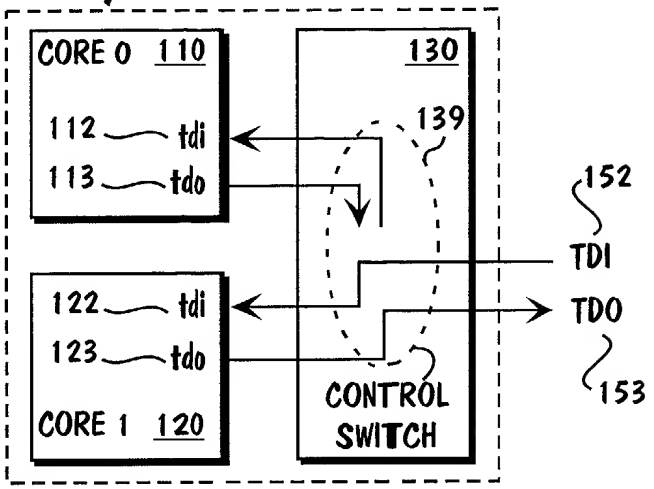


FIG. 3b



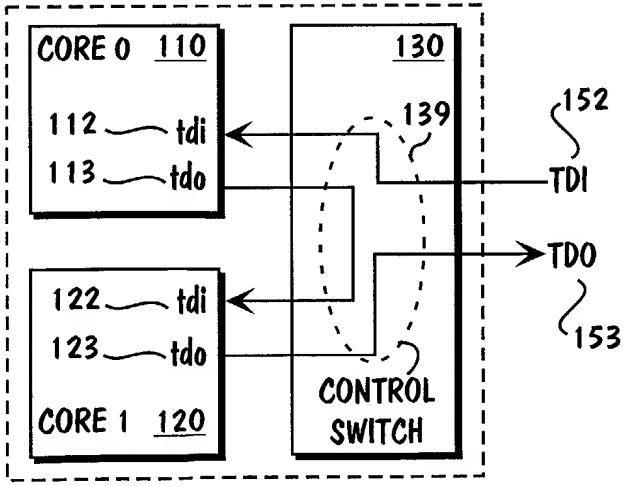


FIG. 3c

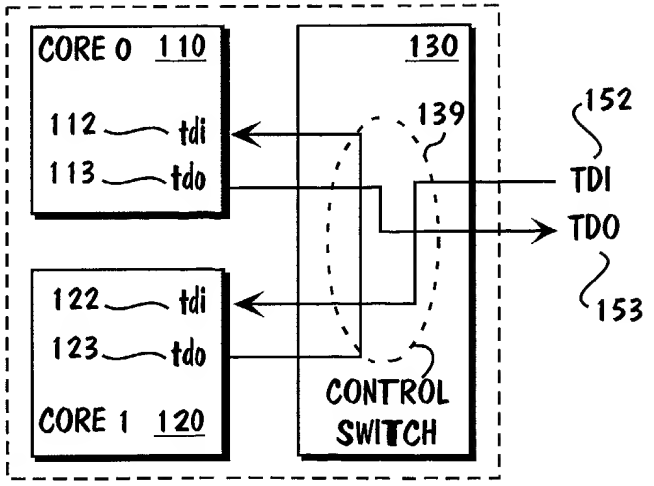


FIG. 3d

FIG. 4a

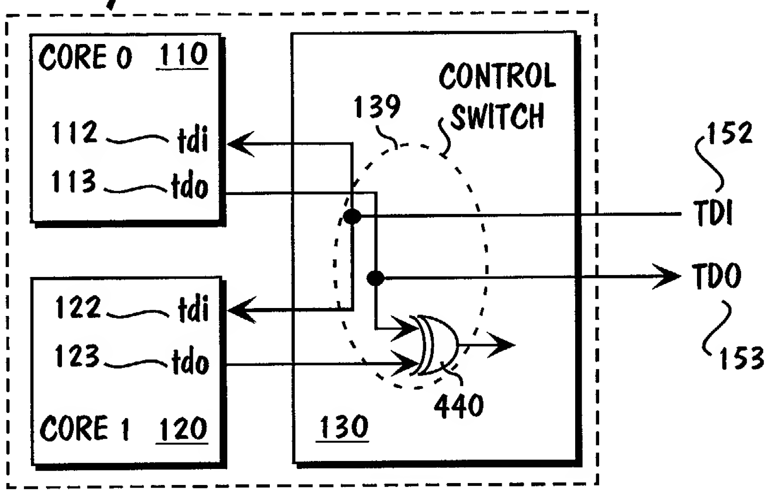
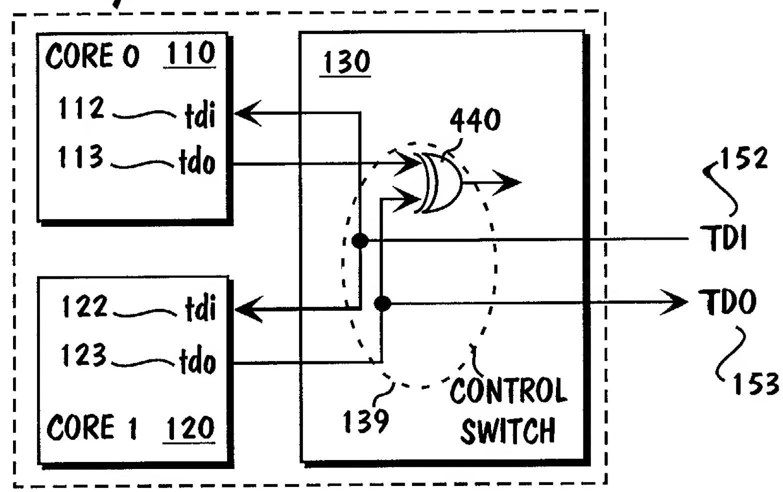


FIG. 4b



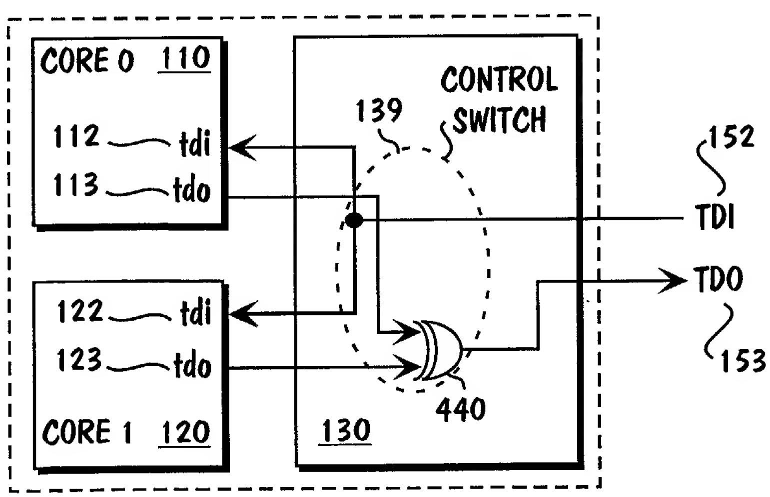


FIG. 4c

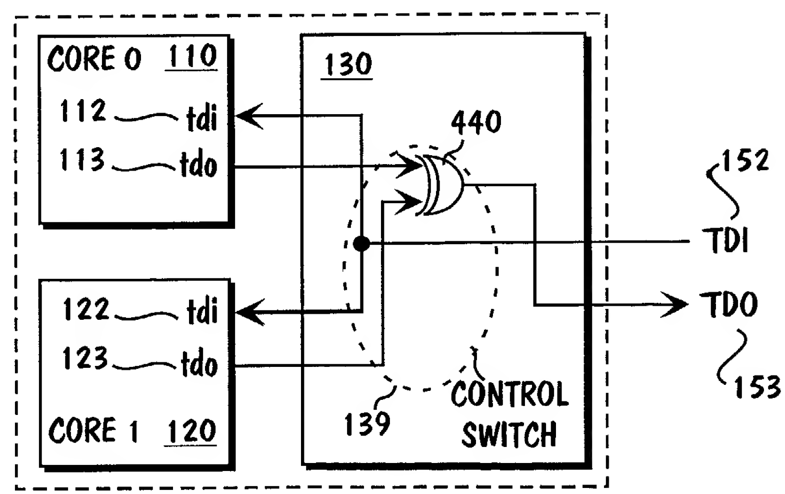


FIG. 4d

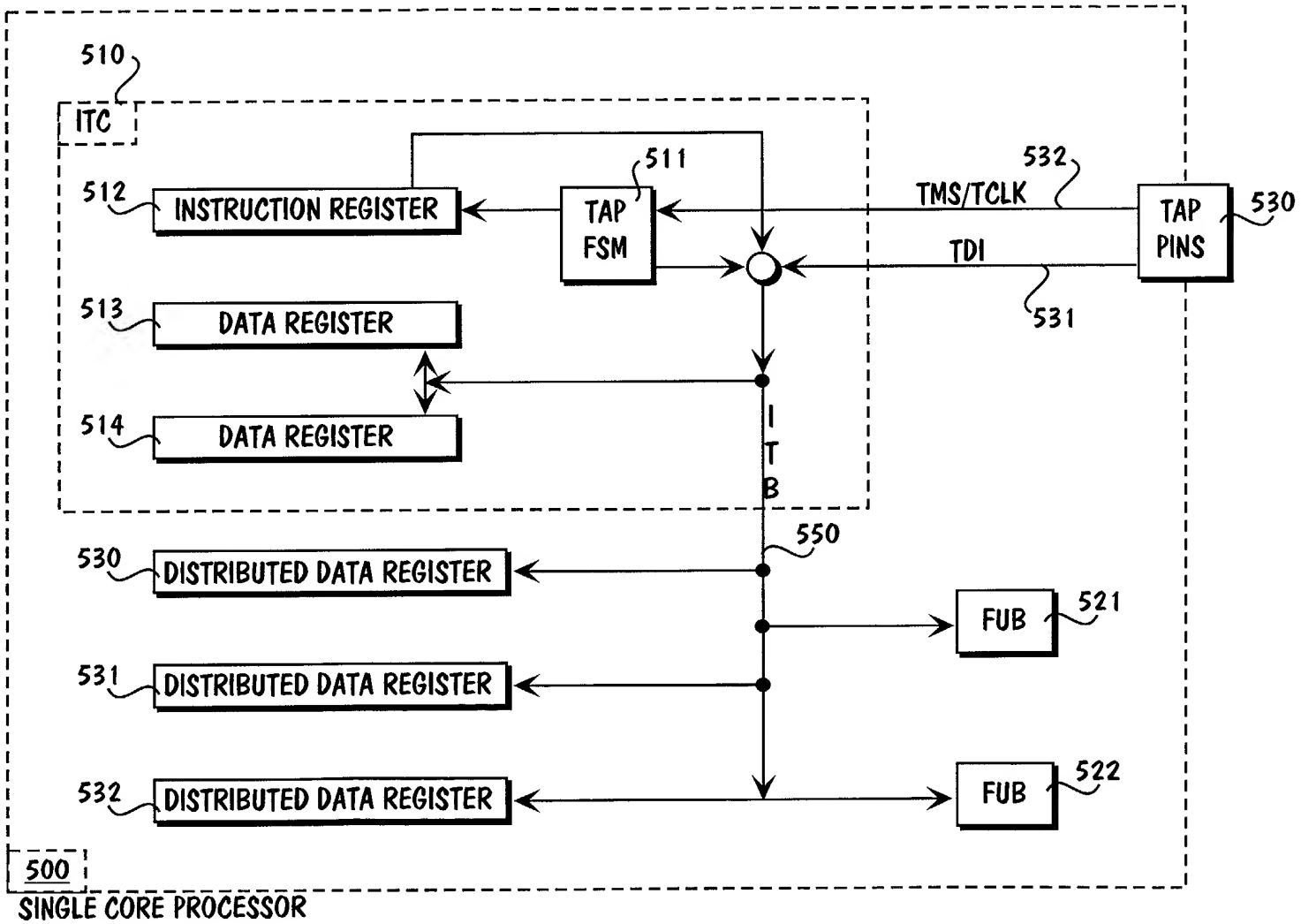

510
ITC
511
512
INSTRUCTION REGISTER
TAP
FSM
532
TMS/TCLK
TAP
PINS
530
TDI
531
513
DATA REGISTER
514
DATA REGISTER
I
T
B
550
530
DISTRIBUTED DATA REGISTER
FUB
521
531
DISTRIBUTED DATA REGISTER
532
DISTRIBUTED DATA REGISTER
FUB
522
500
SINGLE CORE PROCESSOR

FIG. 5

INTEGRATED TEST BUS

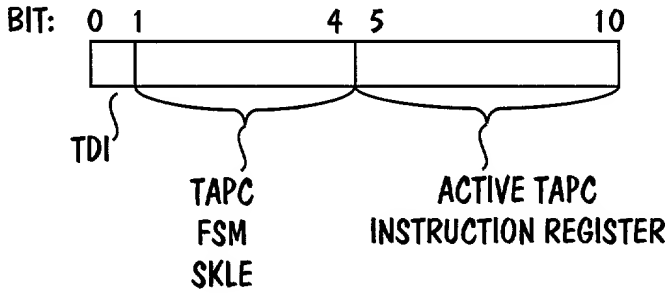


FIG. 6

TAP CORE CONFIGURATION REGISTER

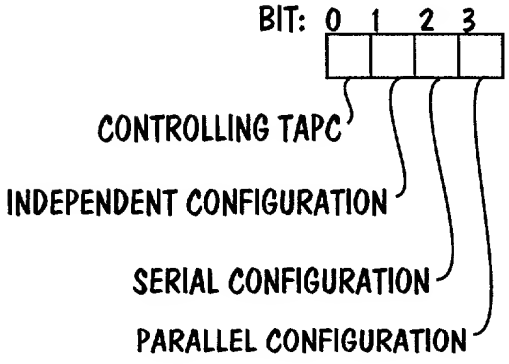


FIG. 7

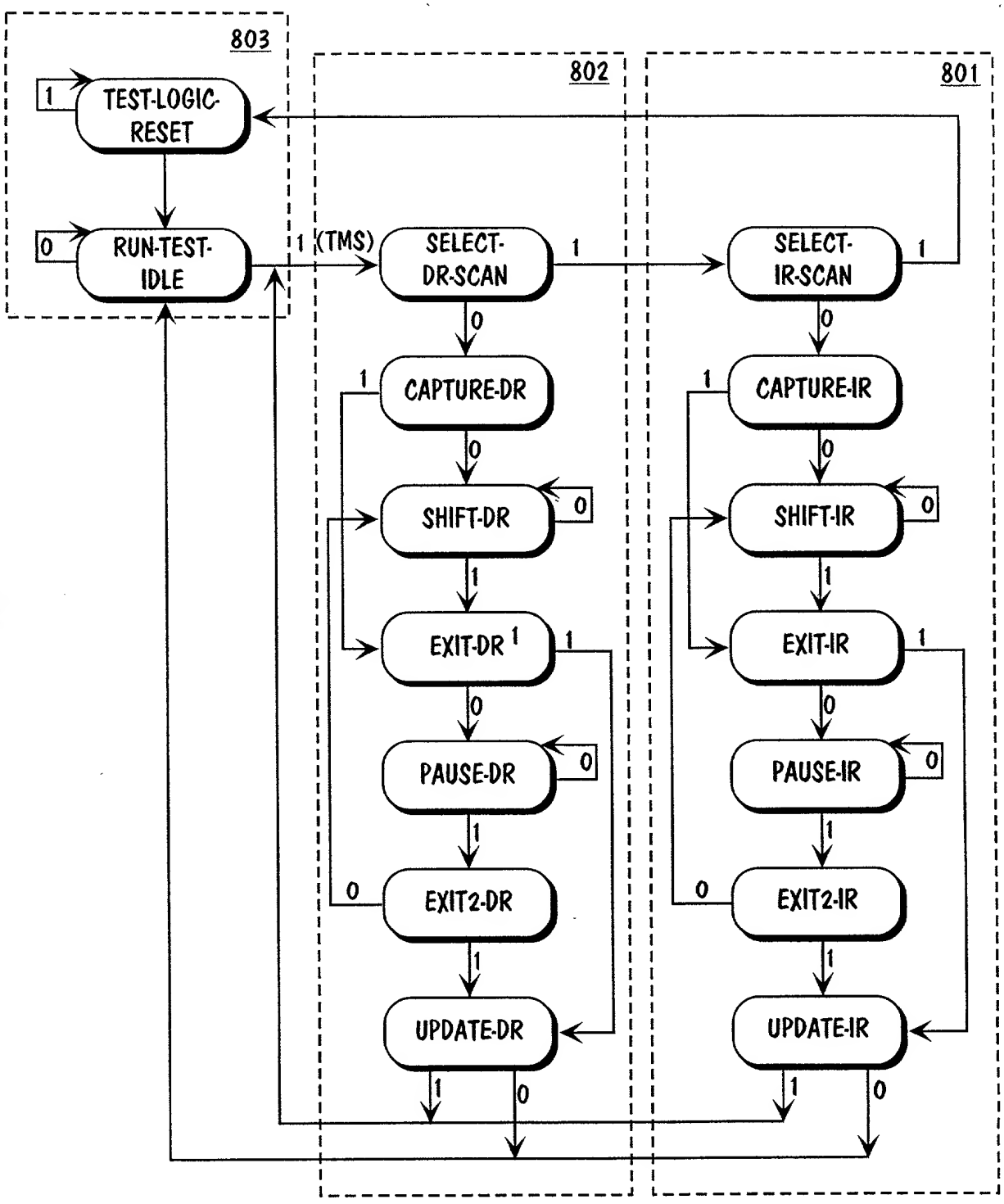

803
802
801
TEST-LOGIC-RESET
RUN-TEST-IDLE
1 (TMS)
SELECT-DR-SCAN
SELECT-IR-SCAN
CAPTURE-DR
CAPTURE-IR
SHIFT-DR
SHIFT-IR
EXIT-DR
EXIT-IR
PAUSE-DR
PAUSE-IR
EXIT2-DR
EXIT2-IR
UPDATE-DR
UPDATE-IR

FIG. 8

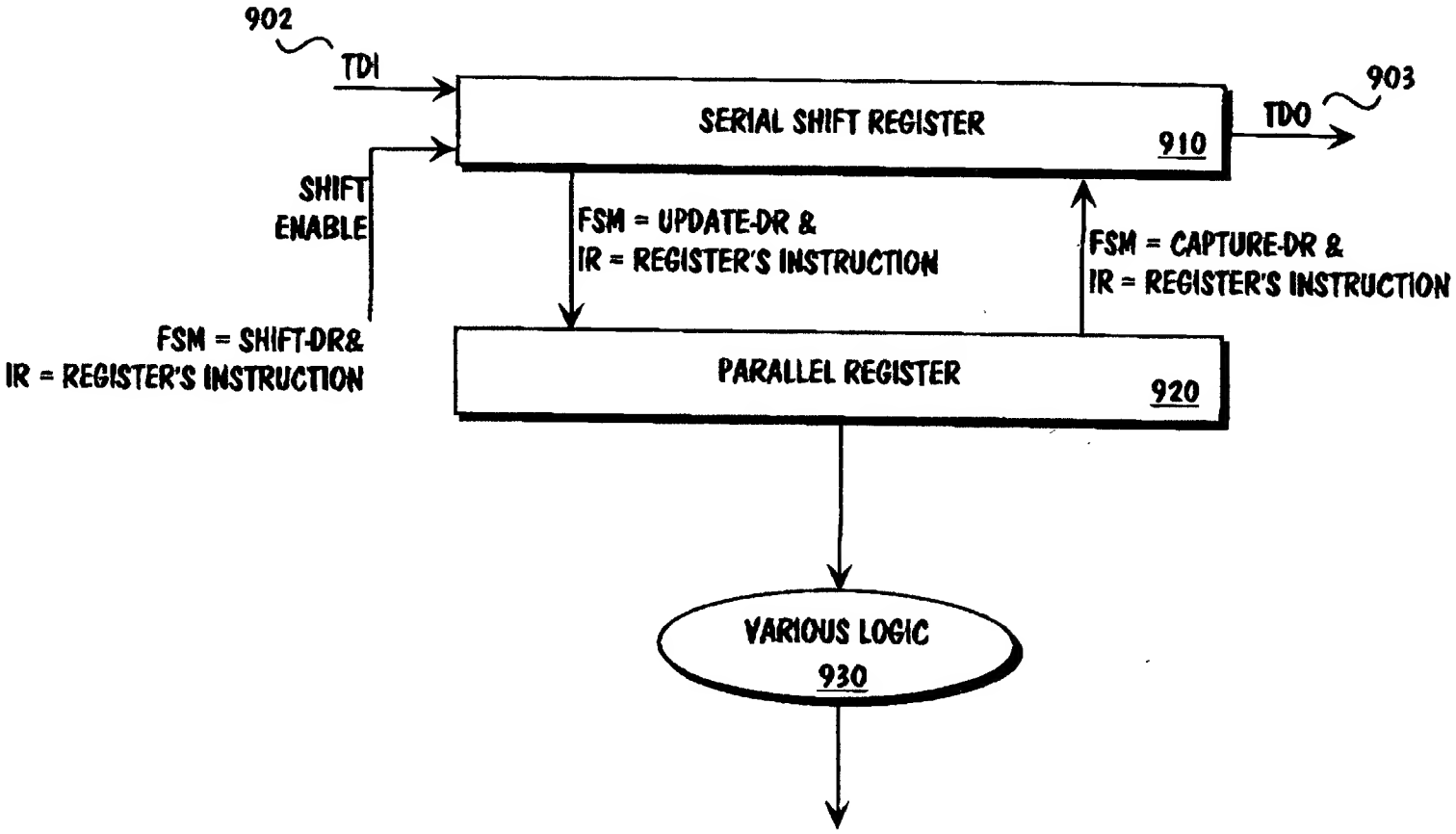


FIG. 9